

What is claimed is:

1. A method for fabricating a semiconductor device, comprising the steps of:

5 (a) forming a plurality of conductive patterns arranged with a predetermined spacing distance on a substrate, each conductive pattern including a conductive layer and a hard mask nitride layer;

(b) forming a planarized inter-layer insulation layer on
10 an entire surface of the resulting structure from the step (a);

(c) etching the inter-layer insulation layer through the use of a wet etching process or a dry etching process so that a height of the inter-layer insulation layer is lower than
15 that of the hard mask nitride layer;

(d) forming an etch stop layer along the inter-layer insulation layer;

(e) forming a self-aligned contact hole of which partial portion expands towards each conductive pattern by etching
20 selectively the etch stop layer and the inter-layer insulation layer until a surface of a partial portion of the substrate disposed within the predetermined spacing distance is exposed and; and

(f) forming a self-aligned contact structure by filling
25 the self-aligned contact hole with a conductive material.

2. The method as recited in claim 1, wherein the etch

stop layer is a nitride-based layer and has a thickness ranging from about 50 Å to about 1000 Å.

3. The method as recited in claim 2, wherein the inter-
5 layer insulation layer is an oxide-based layer.

4. The method as recited in claim 1, wherein the hard mask nitride layer has a thickness in a range from about 1000 Å to about 5000 Å.

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5. The method as recited in claim 4, wherein at the step of etching the inter-layer insulation layer, the inter-layer insulation layer is etched from an upper part of the hard mask nitride layer until reaching a thickness in a range from about
15 300 Å to about 1500 Å.

6. The method as recited in claim 5, wherein the inter-layer insulation layer is made of any material selected from a group consisting of a boron-phosphorus silicate glass (BPSG),
20 high temperature oxide (HTO), medium temperature oxide (MTO), high density plasma (HDP) oxide, tetra-ethyl-ortho silicate (TEOS) and advanced planarization layer (APL).

7. The method as recited in claim 1, wherein the
25 conductive layer is a bit line and the conductive material is a storage node contact plug.

8. The method as recited in claim 1, wherein the self-aligned contact hole is formed with use of a photoresist pattern formed by employing a photo-exposure process using a light source of KrF or ArF.

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9. The method as recited in claim 1, wherein the storage node contact hole is formed by a self-aligned contact (SAC) process.

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10. The method as recited in claim 9, wherein such gas as C_3F_8 , C_4F_8 , C_5F_8 , C_3F_3 , C_4F_6 or C_2F_4 is used as a main etch gas to provide high etch selectivity during the SAC process.

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11. The method as recited in claim 9, wherein during the SAC process, such gas as CHF_3 , C_2HF_5 , CH_2F_2 or CH_3F is also used as the etch gas for increasing a bottom side area of the storage node contact hole in order to improve reliability of the etch process along with the high etch selectivity.

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12. The method as recited in claim 9, wherein during the SAC process, oxygen gas or Ar gas is also used as the etch gas for improving a stopping function of the etch process by increasing plasma stability and sputtering efficiency.

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13. The method as recited in claim 8, wherein a mask for forming the storage node contact hole is formed in a hole-

type, T-type or a line-type.